IN THE CLAIMS

1-8. (canceled)

9. (Previously presented) A method of operating a ROM embedded DRAM, comprising:
receiving a row and column address to read data from a ROM section;
reading an encoded ROM bit;
correcting the read ROM bit if necessary with on-chip error correcting circuitry; and
presenting the corrected ROM bit as output data.

10. (Previously presented) The method of claim 9, wherein correcting comprises:
decoding the read ROM bit with the on-chip error correcting circuitry;
comparing the decoded ROM bit with the actual ROM bit; and
correcting if the decoded ROM bit differs from the read ROM bit.

11. (Previously presented) The method of claim 10, wherein decoding comprises:
error correcting with ECC circuitry.

12. (original) The method of claim 11, wherein error correcting with ECC circuitry comprises:
generating an ECC corrected ROM bit from a read ROM bit;
comparing the ECC corrected bit with the read ROM bit; and
correcting the read ROM bit if the ECC corrected ROM bit and the read ROM bit do not match.

13. (original) The method of claim 10, wherein decoding comprises:
error correcting with parity checking.

14. (original) The method of claim 13, wherein error correcting with parity checking comprises:
comparing the parity check bit with the read ROM bit; and
inverting the read ROM bit if the parity bit indicates an error.

15-23. (canceled)

24. (Previously presented) A method of operating a ROM embedded DRAM, comprising:

receiving a row and column address to read data from a ROM section;

reading a byte of ROM data using an on-chip error correcting code decoder;

correcting the read ROM bit if necessary; and

presenting the corrected ROM bit as output data.

25. (original) The method of claim 24, wherein reading a byte of ROM data using error correcting code comprises:

reading a byte of ROM data;

decoding the byte of ROM data; and

determining if the ROM data is correct.

26. (Previously presented) The method of claim 25, wherein decoding is performed by on-chip decoding circuitry chosen from a groups consisting of:

parity, Hamming code, modified Hamming code, Gray code, polynomial checking, and cyclical redundancy checking.